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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDREJ S. MITROVIC

Appeal 2009-008022
Application 10/673,138
Technology Center 2100

Decided: March 3, 2010

Before JAMES D. THOMAS, LANCE LEONARD BARRY, and STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-40 and 44-46. Claims 41-43 and 47 have been cancelled. We have jurisdiction under 35 U.S.C. § 6(b).

The Invention

The disclosed invention relates generally to first principles simulation in semiconductor manufacturing processes (Spec. 1).

Independent claim 1 is illustrative:

> 1. A method of facilitating a process performed by a semiconductor processing tool, comprising:
>
> inputting process data related to an actual process being performed by the semiconductor processing tool;
>
> inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
>
> performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and
>
> using the first principles simulation result obtained during performance of the actual process to facilitate the actual process being performed by the semiconductor processing tool.

The References

The Examiner relies upon the following references as evidence in support of the rejections:

Sonderman	US 6,802,045 B1	Oct. 05, 2004 (filed Apr. 19, 2001)

V. K. Jain and A. D. Snyder, *Mathematic-Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena*,

1994 Int'l Symposium on Parallel Architectures, Algorithms and Networks (ISPAN), 366-373 (IEEE, 1994) ("Jain").

The Rejections

The Examiner rejects claims 1-40 and 44-46 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman and Jain.

ISSUE

Appellant argues that Sonderman fails to disclose or suggest "performing first principles simulation *for the actual process being performed during performance of the actual process*" (App. Br. 16).

Did Appellant demonstrate that the Examiner erred in finding that Sonderman discloses or suggests performing a simulation of an actual process during performance of the actual process?

FINDINGS OF FACT

The following Findings of Facts (FF) are shown by a preponderance of the evidence.

1. Sonderman discloses "a method and an apparatus for implementing a control simulation environment into a manufacturing environment" (Abstract).
2. Sonderman discloses a "process control environment 180, a manufacturing/processing environment 170, and a simulation environment 210" (col. 4, ll. 49-51).

3. Sonderman discloses that the "simulation environment 210 allows for testing various manufacturing factors in order to study and evaluate the interaction between the manufacturing factors" (col. 4, ll. 59-61).
4. Sonderman discloses that the "manufacturing environment 170 can send metrology data results into the simulation environment 210" and that the "simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide . . . modified control parameters to the process control environment 180" (col. 5, ll. 1-6).
5. Sonderman discloses that the "process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers" (col. 5, ll. 7-10).

PRINCIPLES OF LAW

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

ANALYSIS

The Examiner finds that Sonderman discloses "performing first principle simulation for the actual process being performed during performance of actual process (Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63; Fig. 1-3)" (Ans. 4). However, Sonderman discloses simulation, process, and manufacturing environments (FF 1) in which the simulation and process environments produce process parameters that the manufacturing environment uses to perform processes (FF 2-3). The manufacturing environment may thus produce metrology data that may be returned to the simulation environment to produce updated process parameters for future processing of semiconductor wafers by the manufacturing environment (FF 4-5). Thus, Sonderman discloses a system in which a simulator (i.e., simulation environment) produces parameters for use in a manufacturing environment (i.e., an "actual process"). Since the manufacturing environment utilizes parameters generated by the simulation environment, the simulation environment must complete processing prior to the performance of the actual process by the manufacturing environment such that the manufacturing environment may utilize the parameters generated by the simulation environment. Therefore, we cannot agree with the Examiner

the Sonderman discloses that the simulation is performed during the performance of the actual process, as recited in claim 1.

The Examiner finds that Sonderman discloses performing a simulation during performance of the actual process because Sonderman discloses that "target values are then used to generate new control inputs, X_{Ti} on line 805 to control a subsequent process of a silicon wafer S_i" (Ans. 10-11; Sonderman, col. 9, ll. 44-46). However, Sonderman discloses applying values to a *subsequent* process. We interpret the term "subsequent" to indicate a process that follows a prior (or current) process. Since the values generated in Sonderman are generated for a subsequent process (i.e., a process to be performed in the future) rather than generating parameters for a process that is currently being performed, we cannot agree with the Examiner's finding.

Claims 21 and 44 recite similar features as claim 1. Accordingly, we conclude that Appellant has met the burden of showing that the Examiner erred in rejecting independent claims 1, 21, and 44 under 35 U.S.C. 103(a), and claims 2-20, 22-40, 45, and 46 which depend therefrom.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellant has demonstrated that the Examiner erred in finding that claims 1-40 and 44-46 would have been obvious to one of ordinary skill.

DECISION

We reverse the Examiner's decision rejecting claims 1-40 and 44-46 as being obvious under 35 U.S.C. § 103.

REVERSED

msc

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